A 2.4V SINGLE SUPPLY PSEUDOMORPHIC MODFET MMIC POWER AMPLIFIER FOR DIGITAL CORDLESS PHONES

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Abstract

A 2.4V single supply pseudomorphic MODFET MMIC power amplifier has been developed for 1.9GHz Japanese Personal Handy-phone System (PHS). The MMIC exhibits very low current of 146mA and low adjacent channel leakage power ratio of –55dBc at output power of 20.5dBm and 2.4V single supply.

Introduction

With increased popularity of portable telephones, GaAs MMICs become widely used in the handsets due to excellent high frequency performances, such as low noise-figure or high power efficiency. Among these GaAs MMICs, single supply MMIC power amplifiers (PA) have been attracted much attention because they can realize very compact and low cost handsets. Several papers have already reported on MMIC-PAs which realize single 3.0V-3.5V supply by the use of MODFETs [1,2]. From the viewpoint of further miniaturization of handsets, there will be strong demands for single supply PAs which can operate below 3.0V in the near future. However, there are few reports on single low voltage (Vd ≦ 2.4V) supply MMIC-PAs [3]. The purpose of this work is to describe the single low voltage operation of a MMIC-PA which has been successfully developed for PHS.

Device and Fabrication

In order to realize single voltage operation, the large amplitude of gate voltage swing and high maximum drain current (Imax) are required for FETs. Therefore, we adopted a double heterojunction pseudo-morphic modulation doped FET (MODFET) to meet above needs. The cross sectional view of the MODFET is shown in Figure 1. The gate metal and its length are Ti/Al/Ti and 0.8μm, respectively. The doping level of two n-AlGaAs layers is $2\times10^{18}(\mathrm{cm}^{-3})$.

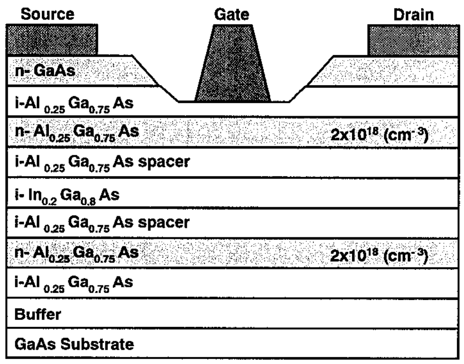


Figure 1. Cross sectional view of the MODFET.

The most essential technical issue of single low voltage supply FETs is how to reduce parasitic resistances due to the surface depletion layer without sacrificing high gate-drain breakdown voltage (BVgd). This is because single supply FETs should be almost in the enhancement mode and electrons in the channel are easily depleted by the surface depletion layer. Therefore, the length of recess region beside the gate is determined to reduce the effect of surface depletion layer [1]. Figures 2 and 3 show DC characteristics of a 3.2mm gate width MODFET. The MODFET exhibits low knee voltage (V_k) of 1.0V, high maximum transconductance (gmmax) of 496mS/mm and high Imax of 1.15A at Vgs=1.0V (359mA/mm) due to the reduction of source and drain parasitic

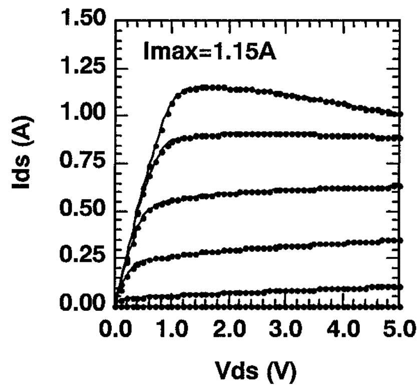


Figure 2. Current-voltage characteristics of the 3.2mm MODFET. (Vgs=0.0V to 1.0V, 0.2V step.)

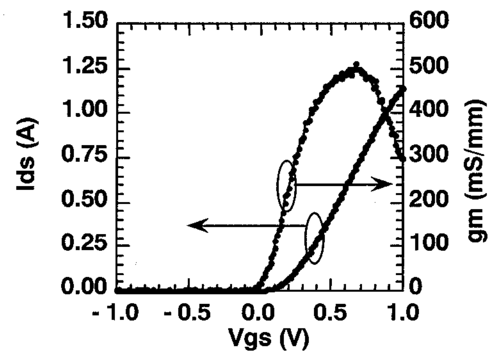


Figure 3. Drain-source current (Ids) and transconductance (gm) versus gate-source voltage (Vgs) characteristics of the 3.2mm MODFET at Vds=2.0V.

resistances. The threshold voltage (Vth) and BVgd are +0.01V and –15V, respectively. As for passive elements in the circuit, spiral inductors are fabricated by Au plating of 3μm. P-SiN film of 2000Å thick is used as an insulator of a MIM capacitor.

MMIC Design

The MMIC using this MODFET is a 3-stage amplifier, as shown in Figure 4. The optimum source and load impedances of a final stage FET are determined by the source-pull/ load-pull measurement at output power (Pout) of 21.5dBm with 1.9GHz $\pi/4$ shift QPSK modulation signal. The matching circuits are designed by nonlinear single tone simulation. The gate widths of three FETs are 200μm, 600μm and 3.2mm, respectively. In order to realize low voltage operation, drain bias circuits are excluded from the chip because the series resistance of the bias circuit is not negligible. Figure 5 shows a photograph of the MMIC chip and its dimension is $0.75 \times 2.00 mm^2$. The MMIC is mounted into a 16-pin flat lead plastic package which has a wide ground pad at the back, as shown in Figure 6. This wide ground pad provides low thermal resistance and low source inductance.

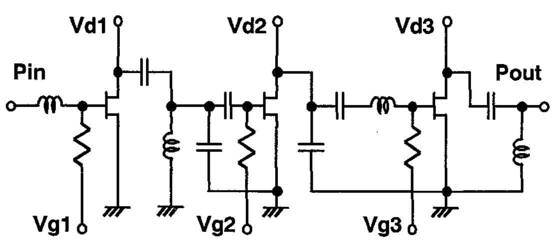


Figure 4. Schematic circuit of a MMIC power amplifier.

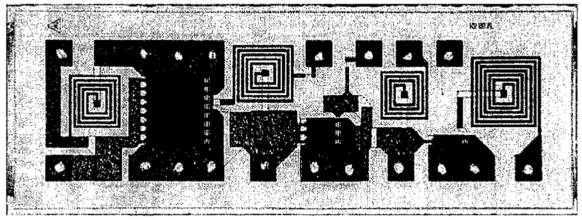
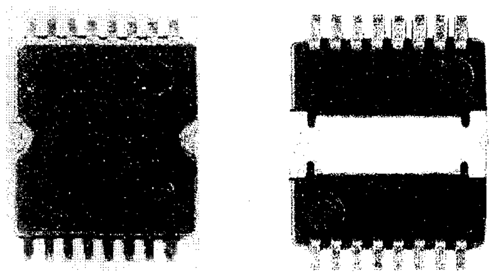


Figure 5. Photograph of the MMIC power amplifier chip.



(a) Face (b) Back

Figure 6. Photographs of a 16-pin flat lead plastic package (SSOF16D).

MMIC Performance

RF performances of the MMIC are evaluated on a test fixture with 1.9GHz $\pi/4$ shift QPSK modulation signal. Drain bias circuits are fabricated on an evaluation board and no external matching is necessary. Figure 7 shows RF performances of the MMIC. Here, gate bias (Vg) is 0.24V and quiescent current is 124mA. The adjacent channel leakage power ratio (ACP) is measured at 600kHz offset point from 1.9GHz. The MMIC achieves very low current of 146mA and low ACP of -55dBc at

Pout=20.5dBm and Vd=2.4V. Gain and power added efficiency (PAE) are 39.8dB and 32.3%, respectively. Due to high Imax and a high Schottky barrier height of the MODFET, gate current (Ig) is less than the measurement limit (|Ig|<2μA) even at large signal output of 20.5dBm.

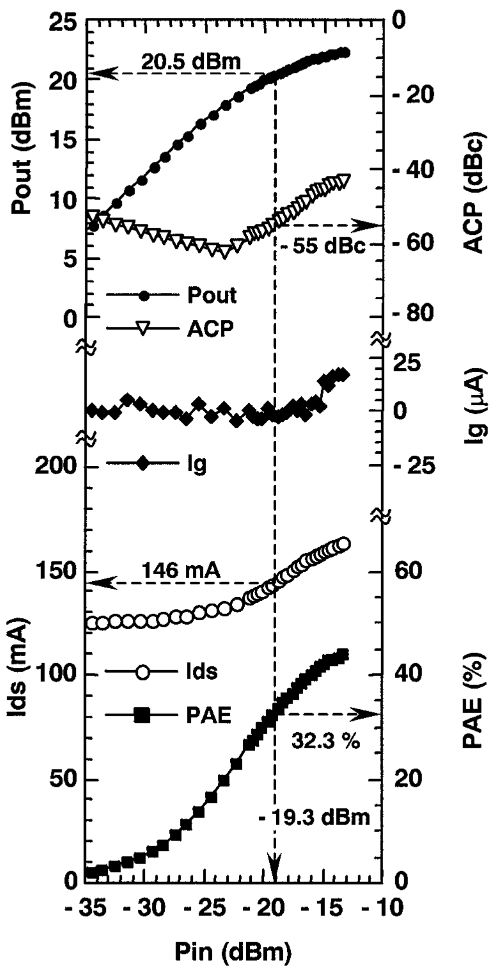


Figure 7. Input-output power performance with adjacent channel leakage power ratio (ACP), gate current (Ig), operating current (Ids) and power added efficiency (PAE) of the MMIC power amplifier at Vd=2.4V and Vg=0.24V.
Input: 1.9GHz π/4 shift QPSK modulation signal.

Conclusion

The single low voltage operation of the pseudomorphic MODFET MMIC power amplifier has been presented. Due to the optimization of the device structure, the MODFET realizes low knee voltage and high maximum drain current with high gate-drain breakdown voltage. Consequently, the MMIC using this MODFET exhibits very low drain current with low adjacent channel leakage power at Pout=20.5dBm and 2.4V single supply.

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